ABSTRACT

In some embodiments, built-in self-test logic is provided for an integrated circuit (IC) device having memory controller logic to generate address and command information for accessing a memory device. Driver circuits are on-chip with the memory controller logic. The driver circuits have outputs that are coupled to on-chip signal pads, respectively. The BIST logic is coupled between the driver circuits and the controller logic. The BIST logic is to transmit, at speed, address and command information that has been generated by the controller logic using the driver circuits in a normal mode of operation for the device. In addition, the BIST logic is able to transmit, at speed, test symbols using the driver circuits in a test mode of operation for the IC device, during which a chip-to-chip connection between the IC device and another device is tested. Other embodiments are also described and claimed.